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EXAMINER
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BHAT, ADITYA S

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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* ANDREW H. BARR, KEN G. POMARANSKI, and DALE J.  
SHIDLA

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Appeal 2009-003190  
Application 10/714,386  
Technology Center 2800

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Decided: May 26, 2010

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Before JOSEPH F. RUGGIERO, KARL D. EASTHOM, and THOMAS S.  
HAHN, *Administrative Patent Judges*.

RUGGIERO, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Final Rejection of claims 1-20, which are all of the pending claims. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Appeal Brief (filed May 20, 2008), the Answer (mailed August, 6, 2008), and the Reply Brief (filed October 6, 2008) for the respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

### *Appellants' Invention*

Appellants' invention relates to the testing of the main memory of a computer system utilizing a test memory card coupled to the input/output (I/O) expansion slot of the computer system. A portion of the main memory of the computer system is tested subsequent to the operating system being booted and during execution of the operating system. Test transactions to an I/O controller coupled to the I/O expansion slot are provided by the test module card causing tests to be performed on the main memory using direct memory access (DMA). (*See generally* Spec. 3:3-11).

Claim 1 is illustrative of the invention and reads as follows:

1. A computer system comprising:
  - a processor configured to execute an operating system;
  - a memory controller coupled to the processor;
  - a memory coupled to the memory controller;
  - a first input/output (I/O) controller coupled to the memory controller;
  - a first expansion slot coupled to the first I/O controller; and
  - a test module card directly coupled to the first expansion slot;wherein the test module card is configured to obtain access to a portion of the memory from the operating system, and wherein the test module card is configured to cause tests to be performed on the portion of

the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory.

### *The Examiner's Rejection*

The Examiner's Answer cites the following prior art references:

Adamane                                      US 2003/0115385 A1                                      Jun. 19, 2003

Merriam-Webster Online Dictionary, Definition of "operating system,"  
retrieved July 9, 2008 from [http://www.merriam-webster.com/dictionary/operating system](http://www.merriam-webster.com/dictionary/operating%20system).<sup>1</sup>

Claims 1-20, all of the pending claims, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Adamane.

### ISSUE

Based on Appellants' contentions, as well as the findings and conclusions of the Examiner, the pivotal issue before us is whether the Examiner erred in determining that Adamane teaches or suggests that a test module obtains access to a portion of memory to be tested from an operating system.

### PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so

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<sup>1</sup> The Merriam-Webster reference is not included as part of the Examiner's rejection of claims, but, rather, is cited as evidence in support of the Examiner's position. (*See Ans. 14-15*).

doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966) (stating that 35 U.S.C. § 103 leads to three basic factual inquiries: the scope and content of the prior art, the differences between the prior art and the claims at issue, and the level of ordinary skill in the art). Furthermore,

‘there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness’ . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

*KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

## ANALYSIS

With respect to the Examiner’s obviousness rejection of appealed independent claims 1, 9, and 15, Appellants’ arguments focus on the alleged deficiency of Adamane in disclosing any interaction between the test modules, i.e., the I/O devices 118 and an operating system. More particularly, Appellants contend (App. Br. 8, 10, and 12; Reply Br. 3-5) that Adamane provides no disclosure of the test module obtaining access to a portion of a computer system from the operating system, a feature present in each of independent claims 1, 9, and 15.

We agree with Appellants. In addressing the language of independent claims 1, 9, and 15, the Examiner has taken the position that all computer systems which perform the function of memory testing require an operating system and, accordingly, the I/O testing devices 118 must interact with an operating system in order to perform the memory test. In support of this

position, the Examiner directs attention (Ans. 10, 13, 14, and 17) to paragraphs [0011] and [0015] of Adamane. We find, however, as also argued by Appellants, no disclosure in these cited paragraphs, or elsewhere within Adamane, of any interaction between the I/O devices 118 and an operating system.

Further, even assuming, *arguendo*, the Examiner's line of reasoning with respect to an operating system in Adamane is correct, this merely establishes the existence of such an operating system in Adamane. We find no evidence, or any valid articulated line of reasoning with a rational underpinning, forthcoming from the Examiner to support the conclusion that the I/O testing devices 118 must *necessarily* obtain access to a portion of the memory being tested from the operation system as claimed, or that an ordinarily skilled artisan would have found it obvious to do so.

To the contrary, evidence on the record before us indicates that there are numerous ways to access a portion of memory being tested other than from an operating system. For example, Appellants' Specification, at page 6, lines 9-17, explains that access to the memory portion to be tested could be obtained, *inter alia*, by sending a request to a memory controller or allocating an unused portion of the memory to be tested. We, therefore, do not sustain the Examiner's 35 U.S.C. § 103(a) rejection of independent claims 1, 9, and 15, nor of claims 2-8, 10-14, and 16-20 dependent thereon.

### CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that Appellants have shown the Examiner erred in rejecting claims 1-20 for obviousness under 35 U.S.C. § 103(a).

### DECISION

The Examiner's 35 U.S.C. § 103(a) rejection of claims 1-20, all of the appealed claims, is reversed.

REVERSED

gvw

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